

CLAIMS

1. A clock signal generation device for generating a clock signal which is synchronous with a reproduced signal from an optical disc on which information is recorded, comprising:

an A/D converting means for sampling the reproduced signal in response to the clock signal and for converting the sampled reproduced signal into a digital value so as to generate a plurality of digital values sequentially in time;

a phase error calculating means for calculating a phase error value indicating a phase error between the reproduced signal and the clock signal based on each of the plurality of digital values;

a loop filter means for outputting a control signal controlling a frequency of the clock signal based on the phase error value;

a clock oscillating means for generating a signal having a frequency corresponding to the control signal as the clock signal; and

a phase error range determining means for determining whether or not the phase error is within a predetermined range based on the phase error value,

wherein the phase error calculating means detects zero-cross points of the plurality of digital values, calculates the phase error value based on a digital value which is closer to the zero level among two digital values between the zero-cross points when it is determined that the phase error is within the predetermined range by the phase error range determining means, and calculates the phase error value based on a digital value which is further from the zero level among the two digital values when it is determined that the phase error is not within the predetermined range by the phase error range determining means.

2. A clock signal generation device according to claim 1, wherein:

the phase error range determining means includes a low-pass filter means for smoothing the phase error value and

the phase error range determining means determines whether or not the phase error is within the predetermined range based on a result of comparison between an output value of the low-pass filter means and a predetermined threshold value.

3. A clock signal generation device according to claim 1, wherein:

the phase error range determining means controls the loop filter means such that a gain of the loop filter means becomes higher when it is determined that the phase error is not within the predetermined range.

4. A clock signal generation device according to claim 1, further

comprising: a synchronization determining means for determining whether or not the reproduced signal and the clock signal are synchronous with each other based on the amplitude of the control signal, and

wherein:

the synchronization determining means makes the determination by the phase error range determining means valid, when it is determined that the reproduced signal and the clock signal are not synchronous with each other, and

the synchronization determining means makes the determination by the phase error range determining means invalid, when it is determined that the reproduced signal and the clock signal are synchronous with each other.

5. A clock signal generation device according to claim 1, further comprising: an offset canceling means for detecting a level at which the digital value is binarized and for canceling an offset component of the digital value based on the level,

wherein the phase error calculating means calculates the phase error value based on the digital value where the offset component of the digital value has been cancelled by the offset canceling means.

6. A clock signal generation device according to claim 5, further comprising: a synchronization determining means for determining whether or not the reproduced signal and the clock signal are in synchronous with each other based on the amplitude of the control signal, and

wherein:

the synchronization determining means controls the offset canceling means such that a gain of the offset canceling means becomes higher, when it is determined that the reproduced signal and the clock signal are not synchronous with each other, and

the synchronization determining means controls the offset canceling means such that a gain of the offset canceling means becomes lower, when it is determined that the reproduced signal and the clock signal are synchronous with each other.

7. A clock signal generation device according to claim 4, further comprising:

an accumulation means for accumulating the digital values over each of predetermined intervals;

an averaging means for averaging the accumulated values by the accumulation means; and

an error detecting means for detecting an error when a difference between the accumulated value by the accumulation means and the average value by the averaging means is larger than a predetermined threshold value,

wherein the synchronization determining means determines that the signals are not synchronous with each other when an error is detected by the error detecting means.

8. A semiconductor integrated circuit used in a clock signal generation device for generating a clock signal which is synchronous with a reproduced signal from an optical disc on which information is recorded, wherein the clock signal generation device includes an A/D converting means for sampling the reproduced signal in response to the clock signal and for converting the sampled reproduced signal into a digital value so as to generate a plurality of digital values sequentially in time; and a clock oscillating means for generating the clock signal,

the semiconductor integrated circuit comprising:

a phase error calculating means for calculating a phase error value indicating a phase error between the reproduced signal and the clock signal based on each of the plurality of digital values;

a loop filter means for outputting a control signal controlling a frequency of the clock signal based on the phase error value; and

a phase error range determining means for determining whether or not the phase error is within a predetermined range based on the phase error value,

wherein:

the phase error calculating means detects zero-cross points of the plurality of digital values, calculates the phase error value based on a digital value which is closer to the zero level among two digital values between the zero-cross points when it is determined that the phase error is within the predetermined range by the phase error range determining means, and calculates the phase error value based on a digital value which is further from the zero level among the two digital values when it is determined that the phase error is not within the predetermined range by the phase error range determining means, and

the clock oscillating means generates a signal having a frequency corresponding to the control signal as the clock signal.

9. A data reproduction method for generating a clock signal which is synchronous with a reproduced signal from an optical disc on which information is recorded and for outputting reproduced data obtained by digitizing the reproduced signal in synchronization with the clock signal, the data reproduction method comprising the steps of:

(a) sampling the reproduced signal in response to the clock signal and converting the sampled reproduced signal into a digital value so as to generate plurality of digital values in the order of time sequence;

(b) calculating a phase error value indicating a phase error between the reproduced signal and the clock signal based on each of the plurality of digital values;

(c) outputting a control signal controlling a frequency of the clock signal based on the phase error value;

(d) generating a signal having a frequency corresponding to the control signal as the clock signal; and

(e) determining whether or not the phase error is within a predetermined range based on the phase error value,

wherein the step (b) includes the steps of:

detecting zero-cross points of the plurality of digital values;

calculating the phase error value based on a digital value which is closer to the zero level among two digital values between the zero-cross points when it is determined that the phase error is within the predetermined range in the phase error range determining step; and

calculating the phase error value based on a digital value which is further from the zero level among the two digital values when it is determined that the phase error is not within the predetermined range in the phase error range determining step.

10. A clock signal generation device for generating a clock signal which is synchronous with a reproduced signal from a disc on which information is recorded, comprising:

an A/D converting means for sampling the reproduced signal in response to the clock signal and for converting the sampled reproduced signal into a digital value so as to generate a plurality of digital values in the order of time sequence;

a first phase error calculating means for calculating a first phase error value indicating a phase error between the reproduced signal and the clock signal based on each of the plurality of digital values;

a first displacement distribution detecting means for detecting a distribution of displacements of the first phase error values;

a loop filter means for generating a control signal controlling a frequency of the clock signal based on the first phase error values and a detection result of the distribution of displacements of the first phase error values; and

a clock oscillating means for generating a signal having a frequency corresponding to the control signal as the clock signal,

wherein the loop filter means generates the control signal such that a deviation of the distribution of displacements of the first phase error values becomes smaller.

11. A clock signal generation device according to claim 10, further comprising:

a synchronization determining means for determining whether or not the reproduced signal and the clock signal are synchronous with each other based on the amplitude of the control signal,

wherein:

the synchronization determining means makes the detection by the first displacement distribution detecting means valid, when it is determined that the reproduced signal and the clock signal are not synchronous with each other, and

the synchronization determining means makes the detection by the first displacement distribution detecting means invalid, when it is determined that the reproduced signal and the clock signal are synchronous with each other.

12. A clock signal generation device according to claim 11, further comprising:

an accumulation means for accumulating the digital values over each of predetermined intervals;

an averaging means for averaging the accumulated values by the accumulation means; and

an error detecting means for detecting an error when a difference between the accumulated value by the accumulation means and the average value by the averaging means is larger than a predetermined threshold value,

wherein the synchronization determining means determines that the signals are not synchronous with each other when an error is detected by the error detecting means.

13. A clock signal generation device according to claim 10, wherein the loop filter means uses only values having polarity where the deviation of the distribution of displacements of the first phase error values becomes smaller, when the deviation of the distribution is large.

14. A clock signal generation device according to claim 10, wherein the displacement distribution detecting means detects the distribution by accumulating signs of the displacements.

15. A clock signal generation device according to claim 14, wherein the displacement distribution detecting means accumulates the signs of the displacements only when the absolute value of the displacement is larger than a predetermined value.

16. A clock signal generation device according to claim 15, wherein the displacement distribution detecting means increases or decreases accumulated values of the signs of the displacements such that the absolute value of the accumulated values becomes smaller, when the absolute value of the displacement is smaller than a predetermined value.

17. A clock signal generation device according to claim 10, further comprising:

a higher frequency band emphasizing filter means for emphasizing a higher frequency band component of a digital value;

a second phase error calculating means for calculating a second phase error value indicating a phase error between the reproduced signal and the clock signal based on an output signal of the higher frequency band emphasizing filter means; and

a second displacement distribution detecting means for detecting a distribution of displacements of the second phase error values,

wherein the loop filter means generates the control signal such that a deviation of the distribution of displacements of the second phase error values becomes smaller.

18. A clock signal generation device according to claim 17, further comprising:

an offset canceling means for detecting a level at which the digital value is binarized and for canceling an offset component of the digital value based on the level,

wherein:

the first phase error calculating means calculates the first phase error value based on the digital value where the offset component of the digital value has been cancelled by the offset canceling means, and

the high frequency band emphasizing filter means is included in the offset canceling means.

19. A clock signal generation device according to claim 18, further comprising:

a synchronization determining means for determining whether or not the reproduced signal and the clock signal are synchronous with each other based on the amplitude of the control signal,

wherein:

the synchronization means controls the offset canceling means such that a gain of the offset canceling means becomes higher, when it is determined that the reproduced signal and the clock signal are not synchronous with each other, and

the synchronization means controls the offset canceling means such that a gain of the offset canceling means becomes lower, when it is determined that the reproduced signal and the clock signal are synchronous with each other.

20. A semiconductor integrated circuit used in a clock signal generation device for generating a clock signal which is synchronous with a reproduced signal from an optical disc on which information is recorded, wherein the clock signal generation device includes an A/D converting means for sampling a reproduced signal in response to a clock signal and for convert the sampled reproduced signal into a digital signal so as to generate a plurality of digital values sequentially in time; and a clock oscillating means for generating the clock signal,

the semiconductor integrated circuit comprising:

a first phase error calculating means for calculating a first phase error value indicating a phase error between the reproduced signal and the clock signal based on each of the plurality of digital values;

a first displacement distribution detecting means for detecting a distribution of displacements of the first phase error values; and

a loop filter means for generating a control signal controlling a frequency of the clock signal based on the first phase error values and a detection result of the distribution of displacements of the first phase error values;

wherein:

the loop filter means generates the control signal such that a deviation of the distribution of displacements of the first error values becomes smaller, and

the clock oscillating means generates a signal having a frequency corresponding to the control signal as the clock signal.

21. A data reproduction method for generating a clock signal which is synchronous with a reproduced signal from an optical disc on which information is recorded and for outputting reproduced data obtained by digitizing the reproduced signal in synchronization with the clock signal, the data reproduction method comprising the steps of:

(a) sampling the reproduced signal in response to the clock signal and converting the sampled reproduced signal into a digital value so as to generate a plurality of digital values in the order of time sequence;

(b) calculating a first phase error value indicating a phase error between the reproduced signal and the clock signal based on each of the plurality of digital values;

(c) detecting a distribution of displacements of the first phase error values;

(d) generating a control signal controlling a frequency of the clock signal based on the first phase error values and a detection result of the distribution of displacements of the first phase error values; and

(e) generating a signal having a frequency corresponding to the control signal as the clock signal,

wherein the step (d) includes the step of generating the control signal such that a deviation of the distribution of displacements of the first phase error values becomes smaller.